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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,813	11/04/2003	Jin Jeon	8054L-205T	4455

7590 09/12/2006

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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,813	JEON ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *77-96* is/are pending in the application.

4a) Of the above claim(s) *1-76* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *77-96* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11-04-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Acknowledgment is made of applicant's claim for domestic priority under U.S.C. 119(e) and 120. Applicant has complied with one or more conditions for receiving the benefit of an earlier filing date under, 35 U.S.C. 119(e) and 120 by making specific reference to the earlier application; in the instant application. However, applicant has failed to provide the status of nonprovisional parent application(s) (whether patented or abandoned) should also be included. Since parent application has become a patent, the expression "now Patent No. _____" should follow the filing date of the parent application.

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Amendment

3. **Status:** Please all the correspondence and replies to all should be addressed to examiner's art unit 2629. Receipt is acknowledged of papers submitted on 11-04-2003 under amendments, which have been placed of record in the file. Claims 77-96 are pending in this action. Claims 1-76 are cancelled. Applicant has cancelled claims 1-76 and added new claims 77-96. Applicant has not introduced any new matters to amended claims; amended and new claims do have support in the original disclosure.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 11-04-2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

6. The abstract of the disclosure is objected to because total word count exceeds 150.

Correction is required. See MPEP § 608.01(b).

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re*

Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 77-96 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-76 of U.S. Patent No. 6,690,347 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: Comparison of Instant application Claims 77-96 to Claims 1-76 of parent applications;

Instant Application Number US 10699813	**Parent Application Number US 10068892; US Patent Number 6,690,347 B2**
89. An display device comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a substrate, the display cell array circuit comprising	65. An LCD comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a transparent substrate, the display cell array circuit

multiple data lines and multiple gate lines, each of the display cell arrays coupled to a corresponding pair of data line and gate line, the gate driving circuit comprising a shift register including multiple stages coupled in cascade fashion, the shift register sequentially selecting the multiple gate lines depending on output signals of the respective stages, the multiple stages having odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal, wherein each of the multiple stages comprises: an input terminal coupled to an output terminal of one of previous stages; an output terminal coupled to a corresponding gate line; a control terminal coupled to a control terminal of one of next stages; a clock terminal into which a corresponding clock signal is inputted; an external input control terminal for	comprising multiple data lines and multiple gate lines, each of the display cell arrays connected to a corresponding pair of data line and gate line, the gate driving circuit comprising a shift register including multiple stages connected in cascade fashion, the multiple stages having a first stage in which a start signal is coupled to an input terminal, the shift register for sequentially selecting the multiple gate lines depending on output signals of the respective stages, the multiple stages having odd stages for receiving a first clock signal, and even stages for receiving a second clock signal having a phase opposite to the first clock signal, wherein each of the multiple stages comprises: an input terminal connected to an output terminal of a previous stage; an output terminal connected to a corresponding gate line; a control terminal connected to a control terminal of a next stage; a clock

receiving an external input control signal; a pull-up section for providing a corresponding one out of the first and second clock signals to the output terminal; a pull-down section for providing a first power voltage to the output terminal; a pull-down driving section coupled to an input node of the pull-down section, for turning off the pull-down section in response to a front edge of the input signal and turning on the pull- down section in response to a front edge of an output signal of one of next stages; and a pull-up driving section provided with a capacitor of which one end is coupled to an input node of the pull-up section and the other end is coupled to the output terminal, and a discharging section for forcibly discharging the capacitor depending on the external input control signal applied to the external input control terminal, the pull-up driving section turning on the pull-up section by charging	terminal into which a corresponding clock signal is inputted; an external input control terminal for receiving an external input control signal; a pull-up means for providing a corresponding one out of the first and second clock signals to the output terminal; a pull-down means for providing a first power voltage to the output terminal; a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to a front edge of the input signal and turning on the pull-down means in response to a front edge of an output signal of a next stage; and a pull-up driving means provided with a capacitor of which one end is connected to an input node of the pull-up means and the other end is connected to the output terminal, and a discharging means for forcibly discharging the capacitor depending on the external input control signal applied to the external

the capacitor in response to the front edge of the input signal and turning off the pull-up section by forcibly discharging the capacitor in response to the front edge of the output signal of one of the next stages.	input control terminal, the pull-up driving means turning on the pull-up means by charging the capacitor in response to the front edge of the input signal and turning off the pull-up means by forcibly discharging the capacitor in response to the front edge of the output signal of the next stage.
85. A shift register in which multiple stages are coupled one after another to each other, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal, each of the multiple stages comprising: an NMOS pull-up transistor of which a first current electrode is coupled to a corresponding clock signal, a control electrode is coupled to a first node, and a second current	39. A shift register in which multiple stages are connected one after another to each other, the multiple stage having a first stage in which a start signal is inputted into an input terminal, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd stages for receiving a first clock signal and even stages for receiving a second clock signal having a phase opposite to the first clock signal, each of the multiple stages comprising: an NMOS pull-up transistor of which drain is connected to a corresponding clock signal,

electrode is coupled to an output terminal; an NMOS pull-down transistor of which a first current electrode is coupled to the output terminal, a control electrode is coupled to a second node and a second current electrode is coupled to a first power voltage; a capacitor coupled between the first node and the output terminal; a first transistor of which a first current electrode is coupled to a second power voltage, a control electrode is coupled to an input signal and a second current electrode is coupled to the first node; a second transistor of which a first current electrode is coupled to the first node, a control electrode is coupled to an output signal of one of next stages and a second current electrode is coupled to the first power voltage; a third transistor of which a first current electrode is coupled to the first node, a control electrode is coupled to the second node and a second current electrode	gate is connected to a first node and source is connected to an output terminal; an NMOS pull-down transistor of which drain is connected to the output terminal, gate is connected to a second node and source is connected to a first power voltage; a capacitor connected between the first node and the output terminal; a first transistor of which drain is connected to a second power voltage, gate is connected to an input signal and source is connected to the first node; a second transistor of which drain is connected to the first node, gate is connected to an output signal of a next stage and source is connected to the first power voltage; a third transistor of which drain is connected to the first node, gate is connected to the second node and source is connected to the first power voltage; a fourth transistor of which drain and gate are commonly connected to the second power voltage and source is connected to

is coupled to the first power voltage; a fourth transistor of which a first current electrode and a control electrode are commonly coupled to a second power voltage and a second current electrode is coupled to the second node; and a fifth transistor of which a first current electrode is coupled to the second node, a control electrode is coupled to the first node and a second current electrode is coupled to the first power voltage.	the second node; and a fifth transistor of which drain is connected to the second node, gate is connected to the first node and source is connected to the first power voltage.

Note the comparison above Claim 89 of instant application to claim 65 of parent application; the language has been changed to avoid 101 statutory double patenting rejections. However, Claim 89 and 65 are claiming same limitation. The both applications, the instant as well as parent application are claiming An LCD comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a transparent substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays connected to a corresponding pair of data line and gate line, the gate driving circuit comprising a shift register including multiple stages connected in cascade fashion, the multiple stages having a

first stage in which a start signal is coupled to an input terminal, the shift register for sequentially selecting the multiple gate lines depending on output signals of the respective stages, the multiple stages having odd stages for receiving a first clock signal, and even stages for receiving a second clock signal having a phase opposite to the first clock signal, wherein each of the multiple stages comprises: an input terminal connected to an output terminal of a previous stage; an output terminal connected to a corresponding gate line; a control terminal connected to a control terminal of a next stage; a clock terminal into which a corresponding clock signal is inputted; an external input control terminal for receiving an external input control signal; a pull-up means for providing a corresponding one out of the first and second clock signals to the output terminal; a pull-down means for providing a first power voltage to the output terminal; a pull-down driving means connected to an input node of the pull-down means, for turning off the pull-down means in response to a front edge of the input signal and turning on the pull-down means in response to a front edge of an output signal of a next stage; and a pull-up driving means provided with a capacitor of which one end is connected to an input node of the pull-up means and the other end is connected to the output terminal, and a discharging means for forcibly discharging the capacitor depending on the external input control signal applied to the external input control terminal, the pull-up driving means turning on the pull-up means by charging the capacitor in response to the front edge of the input signal and turning off the pull-up means by forcibly discharging the capacitor in response to the front edge of the output signal of the next stage. The comparison of instant application claim 85 to parent application claim 39 are claiming shift registers and it comprising of multistage NMOS transistors with their specific

connectivity's. Similar argument can be made to rest of the dependent as well as independent claims of instant application comparing with parent application.

Response to Arguments

9. Applicant's arguments, see remarks, filed 11-04-2003, with respect to the amendments are persuasive. The claims 1-76 has been cancelled and newly added claims 77-96 are pending.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

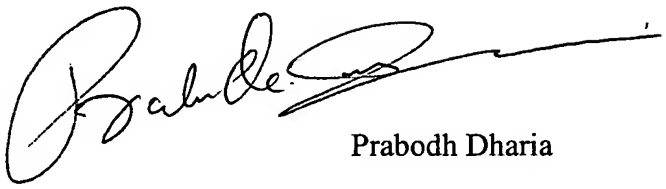
11. The fax phone number for the organization where this application or proceeding is assigned is 573-272-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231



Prabodh Dharia

Partial Signatory Authority Program

AU2629

September 8, 2006